WHAT IS CLAIMED IS:

1. A circuit fabricated in an integrated circuit with a differential input and a differential output, the circuit comprising:

a differential circuit with a first NMOS transistor and a second NMOS transistor, where the first NMOS transistor has a source, a gate, and a drain, and the second NMOS transistor has a source, a gate, and a drain, where the source of the first NMOS transistor and the source of the second NMOS transistor are coupled, where the gate of the first NMOS transistor and the gate of the second NMOS transistor are configured to receive the differential input, and where the drain of the first NMOS transistor and the drain of the second NMOS transistor are configured to provide the differential output;

a first current source with at least a first terminal, where the first terminal of the first current source is coupled to the source of the first NMOS transistor and to the source of the second NMOS transistor;

a first active load with at least a first terminal coupled to the drain of the first NMOS transistor of the differential circuit, where the first terminal of the first active load has an inductive impedance characteristic as seen from the drain of the first NMOS transistor; and

a second active load coupled to the drain of the second NMOS transistor of the differential circuit, where the second active load has an inductive impedance characteristic as seen from the drain of the second NMOS transistor.

2. The circuit as defined in Claim 1, where the first current source is an NMOS transistor with a source, a gate, and a drain, and where the first terminal of the first current source corresponds to the drain of the NMOS transistor.

3. The circuit as defined in Claim 1, wherein the first active load and the second active load exhibit the inductive impedance characteristic without benefit of a passive inductor.

4. The circuit as defined in Claim 1, wherein the first active load further comprises:

a third NMOS transistor with a source, a gate, and a drain, where the source corresponds to the first terminal of the first active load, where the drain is coupled to a first voltage reference; and

a resistance device with a first terminal and a second terminal, where the first terminal of the resistance device is coupled to the gate of the third NMOS transistor, and where the second terminal of the resistance device is coupled to a second voltage reference.

5. The circuit as defined in Claim 4, wherein the first active load further comprises a capacitor with a first terminal and a second terminal, where the first terminal of the capacitor is coupled to the gate of the third NMOS transistor, and where the second terminal of the capacitor is coupled to the source of the third NMOS transistor.

6. The circuit as defined in Claim 4, further comprising a delta-V_{GS} bias that is coupled to the second voltage reference.

7. The circuit as defined in Claim 4, wherein the first active load corresponds to a tunable active load, and where the resistance device corresponds to a device with a controllable resistance.

8. The circuit as defined in Claim 7, wherein the resistance device corresponds to a fourth NMOS transistor with a source, a gate, and a drain, where the source of the fourth NMOS transistor corresponds to the first terminal of the resistance device, where the drain of the fourth NMOS transistor corresponds to the second terminal of the resistance device, and where the gate of the fourth NMOS transistor corresponds to a control terminal for the controllable resistance.

9. The circuit as defined in Claim 4, wherein the resistance device corresponds to a polysilicon resistor.

10. The circuit as defined in Claim 1, wherein the first active load further comprises:

a PMOS transistor with a source, a gate, and a drain, where the drain corresponds to the first terminal of the first active load, and where the source is coupled to a first voltage reference;

a resistance device with a first terminal and a second terminal, where the first terminal of the resistance device is coupled to the gate of the PMOS transistor, and where the second terminal of the resistance device is coupled to the drain of the PMOS transistor; and

a second current source with at least a first terminal coupled to the gate of the PMOS transistor and to the first terminal of the resistance device.

11. The circuit as defined in Claim 10, wherein the first active load further comprises a capacitor with a first terminal and a second terminal, where the first terminal of the capacitor is coupled to the gate of the PMOS transistor, and where the second terminal of the capacitor is coupled to the source of the PMOS transistor.

12. The circuit as defined in Claim 1, further comprising:

a second current source coupled to the drain of the first NMOS transistor of the differential circuit; and

a third current source coupled to the drain of the second NMOS transistor of the differential circuit.

13. The circuit as defined in Claim 12, wherein:

the second current source further comprises a first series combination of a first small NMOS transistor and a first large NMOS transistor, where the first small NMOS transistor is disposed in the current path between the drain of the first NMOS transistor and a drain of the first large NMOS transistor, where a gate of the first small NMOS transistor is coupled to a voltage reference, and where the first large NMOS transistor is configured as a current source; and

the third current source further comprises a second series combination of a second small NMOS transistor and a second large NMOS transistor, where the second small NMOS transistor is disposed in the current path between the drain of the second

NMOS transistor and a drain of the second large NMOS transistor, where a gate of the second small NMOS transistor is coupled to a voltage reference, and where the second large NMOS transistor is configured as a current source.

14. The circuit as defined in Claim 1, further comprising:

a third NMOS transistor with a source, a gate, and a drain, where the drain of the third NMOS transistor is coupled to the drain of the first NMOS transistor, and where the gate of the third NMOS transistor is coupled to the gate of the first NMOS transistor;

a fourth NMOS transistor with a source, a gate, and a drain, where the drain of the fourth NMOS transistor is coupled to the drain of the second NMOS transistor, and where the gate of the fourth NMOS transistor is coupled to the gate of the second NMOS transistor;

at least one capacitive device with at least a first terminal and a second terminal, where the first terminal of the at least one capacitive device is coupled to the source of the third NMOS transistor, and where the second terminal of the at least one capacitive device is coupled to the source of the fourth NMOS transistor;

a second current source with at least a first terminal, where the first terminal of the second current source is coupled to the source of the third NMOS transistor and to the first terminal of the at least one capacitive device; and

a third current source with at least a first terminal, where the first terminal of the third current source is coupled to the source of the fourth NMOS transistor and to the second terminal of the at least one capacitive device.

15. The circuit as defined in Claim 14, wherein the at least one capacitive device corresponds to a capacitor with first terminal and a second terminal, where the first terminal of the capacitor corresponds to the first terminal of the at least one capacitive device and where the second terminal of the capacitor corresponds to the second terminal of the at least one capacitive device.

16. The circuit as defined in Claim 14, wherein the at least one capacitive device corresponds to a first capacitor with a first terminal and a second terminal and to a second capacitor with a first terminal and a second terminal, where the first terminal of the first

capacitor corresponds to the first terminal of the at least one capacitive device, where the first terminal of the second capacitor corresponds to the second terminal of the at least one capacitive device, and where the second terminal of the first capacitor and the second terminal of the second capacitor are coupled to a voltage reference.

17. The circuit as defined in Claim 16, wherein the voltage reference is ground.

18. A digital circuit, comprising:

first and second n-channel devices with their source terminals coupled to a first node, with their gate terminals coupled to receive a first pair of differential logic signals, respectively, and with their drain terminals coupled to a true output and to a complementary output, respectively;

third and fourth n-channel devices with their source terminals coupled to a second node, with their gate terminals coupled to receive a second pair of differential logic signals, and with their drain terminals coupled to the true output and to the complementary output, respectively;

first and second active loads respectively coupling the true output and the complementary output, respectively, to a voltage reference, where the first and second loads exhibit an inductive impedance characteristic without inclusion of an explicit inductor;

a first select n-channel device having a drain terminal coupled to the first node, a gate terminal coupled to receive a first select logic signal, and a source terminal; and

a second select n-channel device having a drain terminal coupled to the second node, a gate terminal coupled to receive a second select logic signal, and a source terminal.

19. The circuit as defined in Claim 18, wherein the first active load further comprises a first resistance device and a first active load n-channel device with a source terminal, a gate terminal, and a drain terminal, where the source of the first active load n-channel device is coupled to the true output, the gate terminal is coupled to the first resistance device, and the drain terminal is coupled to the voltage reference, and where the second active load further comprises a second active load n-channel device with a source terminal, a

gate terminal, and a drain terminal, where the source terminal of the second active load n-channel device is coupled to the complementary output, the gate terminal is coupled to the second resistance device, and the drain terminal is coupled to the voltage reference.

20. The circuit as defined in Claim 18, wherein the n-channel devices correspond to n-channel metal-oxide-semiconductor field-effect transistors (MOSFETs).

21. A current-controlled metal-oxide-semiconductor field-effect transistor (MOSFET) flip-flop circuit, comprising:

a first clocked latch comprising:

first and second NMOS transistors with their source terminals coupled together, with their gate terminals coupled to receive a differential logic signal, and with their drain terminals coupled to a first intermediate output and to a second intermediate output, respectively;

a first clocked NMOS transistor with a drain terminal coupled to the source terminals of the first and second NMOS transistors, with a gate terminal coupled to a first clock signal, and having a source terminal;

third and fourth NMOS transistors with their source terminals coupled together, with their gate terminals and drain terminals respectively cross-coupled to the first intermediate output and to the second intermediate output;

a second clocked NMOS transistor having a drain terminal coupled to the source terminals of the third and fourth NMOS transistors, a gate terminal coupled to a second clock signal, and a source terminal;

first and second active load circuits respectively coupling the first intermediate output and the second intermediate output to a voltage reference, where the first and second active load circuits exhibit an inductive impedance characteristic without inclusion of an explicit inductor;

a second clocked latch comprising:

fifth and sixth NMOS transistors with their source terminals coupled together, with their gate terminals coupled to receive the first intermediate output and the second intermediate output, respectively, and with their drain

terminals coupled to a first flip-flop output and to a second flip-flop output, respectively, where the first flip-flop output and the second flip-flop output correspond to outputs of the flip-flop circuit;

a third clocked NMOS transistor with a drain terminal coupled to the source terminals of the fifth and sixth NMOS transistors, with a gate terminal coupled to the first clock signal, and having a source terminal;

seventh and eighth NMOS transistors with their source terminals coupled together, and with their gate terminals and drain terminals respectively cross-coupled to the first flip-flop output and to the second flip-flop output;

a fourth clocked NMOS transistor with a drain terminal coupled to the source terminals of the seventh and eighth NMOS transistors, with a gate terminal coupled to the second clock signal, and having a source terminal; and

third and fourth active load circuits respectively coupling the first flip-flop output and the second flip-flop output to the voltage reference, where the third and fourth active load circuits exhibit an inductive impedance characteristic without inclusion of an explicit inductor.

22. An integrated circuit with metal-oxide-semiconductor field-effect transistors (MOSFETs) fabricated on a silicon substrate, the integrated circuit comprising at least an input circuit implemented with current-controlled complementary metal-oxide semiconductor field-effect transistor circuits configured with active loads, where the active loads mimic the response of inductors without inclusion of an explicit inductor, where the input circuit is configured to receive an input signal at a first data rate, where the first circuit is configured to generate a first output signal with two or more data lines that operates at a data rate that is slower than the first data rate.

23. The integrated circuit as defined in Claim 22, further comprising a rail-to-rail complementary metal-oxide semiconductor (CMOS) logic circuit coupled to receive the first output signal, where the rail-to-rail CMOS logic circuit is further configured to process data carried by the first output signal and is further configured to generate a second output signal.

24. The integrated circuit as defined in Claim 23, wherein the rail-to-rail CMOS logic circuit is further configured to generate the second output signal such that the second output signal is provided in two or more data lines.

25. The integrated circuit as defined in Claim 24, further comprising an output circuit implemented with current-controlled complementary metal-oxide semiconductor configured with active loads, where the active loads mimic the response of inductors without inclusion of an explicit inductor, where the output circuit is configured to receive the second output signal from the rail-to-rail CMOS logic circuit as an input, where the output circuit is further configured to generate a third output signal at a third data rate that is higher than a data rate of at least one of the two or more data lines of the second output.

26. The integrated circuit as defined in Claim 25, wherein the third data rate and the first data rate are the same.

27. The integrated circuit as defined in Claim 25, wherein the integrated circuit is embodied in a data serialization and deserialization (SERDES) circuit.

28. The integrated circuit as defined in Claim 25, wherein a circuit embodying an active load comprises:

an NMOS transistor with a source, a gate, and a drain, where the source corresponds to a terminal that provides an inductive response, where the drain is coupled to a first voltage reference; and

a resistance device with a first terminal and a second terminal, where the first terminal of the resistance device is coupled to the gate of the NMOS transistor, and where the second terminal of the resistance device is coupled to a second voltage reference.

29. A digital circuit comprising:

a differential circuit with a first NMOS transistor and a second NMOS transistor, where the first NMOS transistor has a source, a gate, and a drain, and the second NMOS transistor has a source, a gate, and a drain, where the source of the first NMOS transistor and the source of the second NMOS transistor are coupled, where the gate of the first NMOS transistor and the gate of the second NMOS transistor are configured to receive a first differential input, and where the drain of the first NMOS

transistor and the drain of the second NMOS transistor are configured to provide the differential output;

a second differential circuit with a third NMOS transistor and a fourth NMOS transistor, where the third NMOS transistor has a source, a gate, and a drain, and where the fourth NMOS transistor has a source, a gate, and a drain, where the source of the third NMOS transistor and the source of the fourth NMOS transistor are coupled, where the gate of the third NMOS transistor and the gate of the fourth NMOS transistor are configured to receive a second differential input, where the drain of the third NMOS transistor is coupled to the source of the first NMOS transistor and to the source of the second NMOS transistor, and where the drain of the fourth NMOS transistor is coupled to the drain of the second NMOS transistor and to part of the differential output;

a current source with at least a first terminal, where the first terminal of the current source is coupled to the source of the third NMOS transistor and to the source of the fourth NMOS transistor;

a first active load with at least a first terminal coupled to the drain of the first NMOS transistor, where the first terminal of the first active load has an inductive impedance as seen from the drain of the first NMOS transistor; and

a second active load coupled to the drain of the second NMOS transistor, where the second active load has an inductive impedance as seen from the drain of the second NMOS transistor.

30. The circuit as defined in Claim 29, wherein the first and second differential inputs and the differential output are arranged such that the circuit corresponds to at least one of an "OR" gate, a "NOR" gate, an "AND" gate, and a "NAND" gate.

31. The circuit as defined in Claim 29, where the current source is an NMOS transistor with a source, a gate, and a drain, and where the first terminal of the first current source corresponds to a drain of the NMOS transistor.

32. The circuit as defined in Claim 29, wherein the first active load and the second active load exhibit the inductive impedance without benefit of a passive inductor.

33. The circuit as defined in Claim 29, wherein the first active load further comprises:

an NMOS transistor with a source, a gate, and a drain, where the source corresponds to the first terminal of the first active load, where the drain is coupled to a first voltage reference; and

a resistance device with a first terminal and a second terminal, where the first terminal of the resistance device is coupled to the gate of the NMOS transistor, and where the second terminal of the resistance device is coupled to a second voltage reference.

34. A digital circuit comprising:

a differential circuit with a first NMOS transistor and a second NMOS transistor, where the first NMOS transistor has a source, a gate, and a drain, and the second NMOS transistor has a source, a gate, and a drain, where the source of the first NMOS transistor and the source of the second NMOS transistor are coupled, where the gate of the first NMOS transistor and the gate of the second NMOS transistor are configured to receive a first differential input for a first differential signal, and where the drain of the first NMOS transistor and the drain of the second NMOS transistor are coupled to the differential output;

a second differential circuit with a third NMOS transistor and a fourth NMOS transistor, where the third NMOS transistor has a source, a gate, and a drain, and where the fourth NMOS transistor has a source, a gate, and a drain, where the source of the third NMOS transistor and the source of the fourth NMOS transistor are coupled, where the gate of the third NMOS transistor and the gate of the fourth NMOS transistor are configured to be responsive to a second differential signal, and where the drain of the third NMOS transistor is coupled to the drain of the first NMOS transistor and to a portion of the differential output, where the drain of the fourth NMOS transistor is coupled to the drain of the second NMOS transistor and to a portion of the differential output;

a third differential circuit with a fifth NMOS transistor and a sixth NMOS transistor, where the fifth NMOS transistor has a source, a gate, and a drain, and

where the sixth NMOS transistor has a source, a gate, and a drain, where the source of the fifth NMOS transistor and the source of the sixth NMOS transistor are coupled, where the gate of the fifth NMOS transistor and the gate of the sixth NMOS transistor are configured to receive a differential input for a third differential signal, where the drain of the fifth NMOS transistor is coupled to the source of the first NMOS transistor and to the source of the second NMOS transistor, where the drain of the sixth NMOS transistor is coupled to the source of the third NMOS transistor and to the source of the fourth NMOS transistor;

a current source with at least a first terminal, where the first terminal of the current source is coupled to the source of the fifth NMOS transistor and to the source of the sixth NMOS transistor;

a first active load with at least a first terminal coupled to the drain of the first NMOS transistor, where the first terminal of the first active load has an inductive impedance as seen from the drain of the first NMOS transistor; and

a second active load coupled to the drain of the second NMOS transistor, where the second active load has an inductive impedance as seen from the drain of the second NMOS transistor.

35. The integrated circuit as defined in Claim 34, wherein the circuit is configured as a multiplexer, wherein the gate of the third NMOS transistor and the gate of the fourth NMOS transistor are coupled to a second differential input to receive the second differential signal, where the first and second differential inputs correspond to inputs for the multiplexer, and where the differential input for the third differential signal corresponds to a select input for the inputs of the multiplexer.

36. The circuit as defined in Claim 34, wherein the circuit is configured as a latch, where the drain of the fourth NMOS transistor is coupled to the gate of the third NMOS transistor and the drain of the third NMOS transistor is coupled to the gate of the fourth NMOS transistor so that the differential output is cross-coupled and provided as an input for the second differential signal for the second differential circuit, where the first differential input corresponds to an input for the latch, and where the differential input for a third differential signal corresponds to a control for the latch.

37. The circuit as defined in Claim 36, wherein the circuit is embodied in a D-type flip-flop (D-FF) cell, wherein a D-FF cell further comprises two circuits configured as latches coupled in series.

38. The circuit as defined in Claim 34, where the current source is an NMOS transistor with a source, a gate, and a drain, and where the first terminal of the first current source corresponds to a drain of the NMOS transistor.

39. The circuit as defined in Claim 34, wherein the first active load and the second active load exhibit the inductive impedance without benefit of a passive inductor.

40. The circuit as defined in Claim 34, wherein the first active load further comprises:

an NMOS transistor with a source, a gate, and a drain, where the source corresponds to the first terminal of the first active load, where the drain is coupled to a first voltage reference; and

a resistance device with a first terminal and a second terminal, where the first terminal of the resistance device is coupled to the gate of the NMOS transistor, and where the second terminal of the resistance device is coupled to a second voltage reference.

41. The circuit as defined in Claim 34, wherein the circuit is embodied in an integrated circuit for data serialization and deserialization (SERDES).

42. An integrated circuit with metal-oxide-semiconductor field-effect transistors (MOSFETs) fabricated on a silicon substrate, the integrated circuit comprising at least a differential logic circuit implemented with current-controlled complementary metal-oxide semiconductor field-effect transistor circuits configured with active loads, and where the active loads mimic the response of inductors without inclusion of an explicit inductor.

43. The integrated circuit as defined in Claim 42, wherein the differential logic circuit is configured to correspond to at least a portion of a buffer, an inverter, an AND gate, a NAND gate, an OR gate, a NOR gate, a multiplexer, a latch, and a flip-flop.